WHAT IS CLAIMED IS:

1. A programmable synchronizer system for effectuating data transfer between first circuitry disposed in a first clock domain and second circuitry disposed in a second clock domain, wherein said first clock domain is operable with a first clock signal and said second clock domain is operable with a second clock signal, said first and second clock signals having a ratio of N first clock cycles to M second clock cycles, where $N/M \geq 1$, comprising:

a first synchronizer controller circuit operating in said first clock domain responsive to a SYNC pulse that is sampled in said first clock domain;

a configuration interface for configuring said first synchronizer controller circuit to compensate for at least one of a variable skew factor and a variable latency factor associated with said first clock signal; and

a second synchronizer controller circuit operating in said second clock domain responsive to a SYNC pulse that is sampled in said second clock domain, said second synchronizer controller circuit operating to generate a plurality of inter-controller control signals towards said first synchronizer controller circuit, wherein each of said first and second synchronizer controller circuits generates a set of synchronizer control signals, a portion of which signals are provided to a first synchronizer operating to control data transfer from said first circuitry to said second circuitry and a portion of which signals are provided to a second synchronizer operating to control data transfer from said second circuitry to said first circuitry.

2. The programmable synchronizer system as recited in claim 1, wherein said SYNC pulse is generated by a phase-locked loop (PLL) when a rising edge in said first clock signal is coincident with a rising edge in said second clock signal.

3. The programmable synchronizer system as recited in claim 1, wherein said first synchronizer comprises:

a first TRANSMIT multiplex-register (MUXREG) block disposed in said first clock domain, said first TRANSMIT MUXREG block operating to transmit a portion of data responsive to a c0_sel control signal that is registered using said first clock signal, wherein said data is generated in said first clock domain by said first circuitry and said c0_sel control signal generated by said first synchronizer controller;

a second TRANSMIT MUXREG block in said first clock domain for transmitting another portion of said data generated in said first clock domain responsive to a c1_sel control signal that is registered using said first clock signal, wherein said c1_sel control signal is generated by said first synchronizer controller; and

a RECEIVE MUXREG block disposed in said second clock domain for receiving said data from said first and second TRANSMIT MUXREG blocks in a serial fashion responsive to a bus_sel control signal that is registered using said second clock signal, wherein said bus_sel control is generated by said second synchronizer controller.

4. The programmable synchronizer system as recited in claim 3, wherein said first TRANSMIT MUXREG block includes a 2:1 MUX that is controlled by said c0_sel control signal.

5. The programmable synchronizer system as recited in claim 3, wherein said second TRANSMIT MUXREG block includes a 2:1 MUX that is controlled by said c1_sel control signal.

6. The programmable synchronizer system as recited in claim 3, wherein said RECEIVE MUXREG block includes a 2:1 MUX that is controlled by said bus_sel control signal.

7. The programmable synchronizer system as recited in claim 3, wherein said data comprises *k*-bit wide data and said first synchronizer includes *k* instances of each of said first and second TRANSMIT MUXREG blocks and said RECEIVE MUXREG block.

8. The programmable synchronizer system as recited in claim 1, wherein said second synchronizer comprises:

a first TRANSMIT multiplex-register (MUXREG) block disposed in said second clock domain, said first TRANSMIT MUXREG block operating to transmit a portion of data responsive to a b0_sel control signal that is registered using said second clock signal, wherein said data is generated in said second clock domain by said second circuitry and said b0_sel control signal is generated by said second synchronizer controller ;

a second TRANSMIT MUXREG block in said second clock domain for transmitting another portion of said data generated in said second clock domain responsive to a b1_sel control signal that is registered using said second clock signal, wherein said b1_sel control signal is generated by said second synchronizer controller; and

a RECEIVE MUXREG block disposed in said first clock domain for receiving said data from said first and second TRANSMIT MUXREG blocks in a serial fashion responsive to a core_sel control signal that is registered using said first clock signal.

9. The programmable synchronizer system as recited in claim 8, wherein said first TRANSMIT MUXREG block includes a 2:1 MUX that is controlled by said b0_sel control signal.

10. The programmable synchronizer system as recited in claim 8, wherein said second TRANSMIT MUXREG block includes a 2:1 MUX that is controlled by said b1_sel control signal.

11. The programmable synchronizer system as recited in claim 8, wherein said RECEIVE MUXREG block includes a 2:1 MUX that is controlled by said core_sel control signal.

12. The programmable synchronizer system as recited in claim 8, wherein said data comprises k-bit wide data and said second synchronizer includes k instances of each of said first and second TRANSMIT MUXREG blocks and said RECEIVE MUXREG block.

13. A programmable synchronizer system for effectuating data transfer across a clock boundary between a core clock domain and a bus clock domain, wherein said core clock domain is operable with a core clock signal and said bus clock domain is operable with a bus clock signal, said core and bus clock signals having a ratio of N core clock cycles to M bus clock cycles, where $N/M \geq 1$, comprising:

first circuit means for synchronizing data transfer from a core clock domain logic block to a bus clock domain logic block;

second circuit means for synchronizing data transfer from said bus clock domain logic block to said core clock domain logic block; and

control means for controlling said first and second circuit means, said control means operating responsive at least in part to configuration means that is configurable based on at least one of skew and latency associated with said core clock signal.

14. The programmable synchronizer system for effectuating data transfer across a clock boundary between a core clock domain and a bus clock domain as recited in claim 13, wherein said first circuit means comprises a core-to-bus synchronizer operable to transfer data from a core clock domain to a bus clock domain, said core clock and bus clock signals having a ratio of 5 core clock cycles to 4 bus clock cycles.

15. The programmable synchronizer system for effectuating data transfer across a clock boundary between a core clock domain and a bus clock domain as recited in claim 13, wherein said second circuit means comprises a bus-to-core synchronizer operable to transfer data from a bus clock domain to a core clock domain, said core clock and bus clock signals having a ratio of 5 core clock cycles to 4 bus clock cycles.

16. The programmable synchronizer system for effectuating data transfer across a clock boundary between a core clock domain and a bus clock domain as recited in claim 13, further including detector means for detecting a phase difference between said core clock and bus clock signals, said detector means operating to generate a control signal directed to said first circuit means.

17. A computer system having a programmable synchronizer apparatus for effectuating data transfer between first circuitry disposed in a first clock domain and second circuitry disposed in a second clock domain, wherein said first clock domain is operable with a first clock signal and said second clock domain is operable with a second clock signal, said first and second clock signals having a ratio of N first clock cycles to M second clock cycles, where $N/M \geq 1$, comprising:

a first synchronizer controller circuit operating in said first clock domain responsive to a SYNC pulse that is sampled in said first clock domain;

a configuration interface for configuring said first synchronizer controller circuit to compensate for at least one of a variable skew factor and a variable latency factor associated with said first clock signal; and

a second synchronizer controller circuit operating in said second clock domain responsive to a SYNC pulse that is sampled in said second clock domain, said second synchronizer controller circuit operating to generate a plurality of inter-controller control signals towards said first synchronizer controller circuit, wherein each of said first and second synchronizer controller circuits generates a set of synchronizer control signals, a portion of which signals are provided to a first synchronizer operating with respect to data transfer from said first circuitry to said second circuitry and a portion of which signals are provided to a second synchronizer operating with respect to data transfer from said second circuitry to said first circuitry.

18. The computer system as recited in claim 17, wherein said SYNC pulse is generated by a phase-locked loop (PLL) responsive to a rising edge in said first clock signal that is coincident with a rising edge in said second clock signal.

19. The computer system as recited in claim 17, wherein said first synchronizer comprises:

a first TRANSMIT multiplex-register (MUXREG) block disposed in said first clock domain, said first TRANSMIT MUXREG block operating to transmit a portion of data responsive to a c0_sel control signal that is registered using said first clock signal, wherein said data is generated in said first clock domain by said first circuitry and said c0_sel control signal generated by said first synchronizer controller;

a second TRANSMIT MUXREG block in said first clock domain for transmitting another portion of said data generated in said first clock domain responsive to a c1_sel control signal that is registered using said first clock signal, wherein said c1_sel control signal is generated by said first synchronizer controller; and

a RECEIVE MUXREG block disposed in said second clock domain for receiving said data from said first and second TRANSMIT MUXREG blocks in a serial fashion responsive to a bus_sel control signal that is registered using said second clock signal, wherein said bus_sel control is generated by said second synchronizer controller.

20. The computer system as recited in claim 19, wherein said first TRANSMIT MUXREG block includes a 2:1 MUX that is controlled by said c0_sel control signal.

21. The computer system as recited in claim 19, wherein said second TRANSMIT MUXREG block includes a 2:1 MUX that is controlled by said c1_sel control signal.

22. The computer system as recited in claim 19, wherein said RECEIVE MUXREG block includes a 2:1 MUX that is controlled by said bus_sel control signal.

23. The computer system as recited in claim 19, wherein said data comprises *k*-bit wide data and said first synchronizer includes *k* instances of each of said first and second TRANSMIT MUXREG blocks and said RECEIVE MUXREG block.

24. The computer system as recited in claim 17, wherein said second synchronizer comprises:

a first TRANSMIT multiplex-register (MUXREG) block disposed in said second clock domain, said first TRANSMIT MUXREG block operating to transmit a portion of data responsive to a b0_sel control signal that is registered using said second clock signal, wherein said data is generated in said second clock domain by said second circuitry and said b0_sel control signal is generated by said second synchronizer controller ;

a second TRANSMIT MUXREG block in said second clock domain for transmitting another portion of said data generated in said second clock domain responsive to a b1_sel control signal that is registered using said second clock signal, wherein said b1_sel control signal is generated by said second synchronizer controller; and

a RECEIVE MUXREG block disposed in said first clock domain for receiving said data from said first and second TRANSMIT MUXREG blocks in a serial fashion responsive to a core_sel control signal that is registered using said first clock signal.

25. The computer system as recited in claim 24, wherein said first TRANSMIT MUXREG block includes a 2:1 MUX that is controlled by said b0_sel control signal.

26. The computer system as recited in claim 24, wherein said second TRANSMIT MUXREG block includes a 2:1 MUX that is controlled by said b1_sel control signal.

27. The computer system as recited in claim 24, wherein said RECEIVE MUXREG block includes a 2:1 MUX that is controlled by said core_sel control signal.

28. The computer system as recited in claim 24, wherein said data comprises *k*-bit wide data and said second synchronizer includes *k* instances of each of said first and second TRANSMIT MUXREG blocks and said RECEIVE MUXREG block.

29. The computer system as recited in claim 17, wherein said first synchronizer is operable to transfer data from a core clock domain that is clocked by a core clock signal operating as said first clock signal to a bus clock domain that is clocked by a bus clock signal operating as said second clock signal, said core clock and bus clock signals having a ratio of 5 core clock cycles to 4 bus clock cycles.

30. The computer system as recited in claim 17, wherein said second synchronizer is operable to transfer data from a bus clock domain that is clocked by a bus clock signal operating as said second clock signal to a core clock domain that is clocked by a core clock signal as operating said first clock signal, said core clock and bus clock signals having a ratio of 5 core clock cycles to 4 bus clock cycles.

31. A programmable synchronizer system for effectuating data transfer between first circuitry disposed in a first clock domain and second circuitry disposed in a second clock domain, wherein said first clock domain is operable with a first clock signal and said second clock domain is operable with a second clock signal, said first and second clock signals having a ratio of N first clock cycles to M second clock cycles, where $N/M \geq 1$, comprising:

a first synchronizer controller circuit operating in said first clock domain responsive to a SYNC pulse that is sampled in said first clock domain;

a configuration interface for configuring said first synchronizer controller circuit to compensate for at least one of a variable skew factor and a variable latency factor associated with said first clock signal; and

a second synchronizer controller circuit operating in said second clock domain responsive to a SYNC pulse that is sampled in said second clock domain and a plurality of inter-controller control signals generated by said first synchronizer controller circuit towards said second synchronizer controller circuit, wherein each of said first and second synchronizer controller circuits generates a set of synchronizer control signals, a portion of which signals are provided to a first synchronizer operating to control data transfer from said first circuitry to said second circuitry and a portion of which signals are provided to a second synchronizer operating to control data transfer from said second circuitry to said first circuitry.

32. The programmable synchronizer system as recited in claim 31, wherein said SYNC pulse is generated by a phase-locked loop (PLL) when a rising edge in said first clock signal is coincident with a rising edge in said second clock signal.

33. The programmable synchronizer system as recited in claim 1, further including detector means for detecting a phase difference between said first clock and second clock signals, said detector means operating to generate a phase detection control signal directed to said first synchronizer controller circuit.